

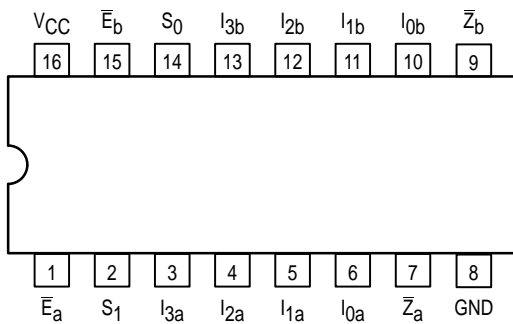


DUAL 4-INPUT MULTIPLEXER

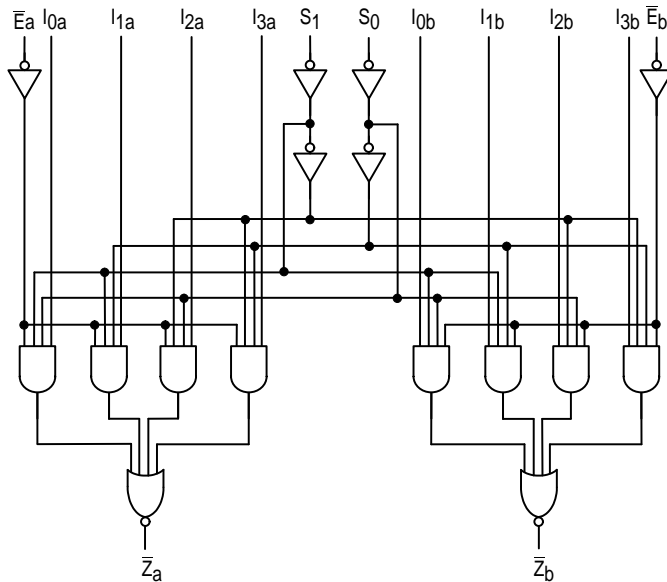
The MC54/74F352 is a very high speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The F352 is the functional equivalent of the F153 except with inverted outputs.

- Inverted Version of the F153
- Separate Enables for Each Multiplexer
- Input Clamp Diode Limits High-Speed Termination Effects

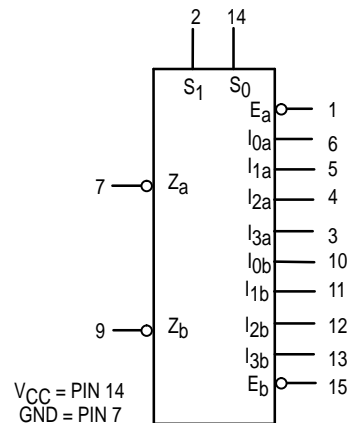
CONNECTION DIAGRAM (TOP VIEW)



LOGIC DIAGRAM



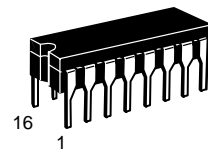
LOGIC SYMBOL



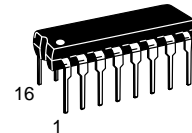
MC54/74F352

DUAL 4-INPUT MULTIPLEXER

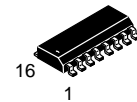
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

MC54/74F352

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	- 55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

FUNCTIONAL DESCRIPTION

The F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S₀, S₁). The two 4-input multiplexer circuits have individual active-LOW Enables (\bar{E}_a , \bar{E}_b) which can be used to strobe the outputs independently. When the Enables (\bar{E}_a , \bar{E}_b) are HIGH, the corresponding outputs (\bar{Z}_a , \bar{Z}_b) are forced HIGH.

The logic equations for the outputs are shown below:

$$\bar{Z}_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot S_1 \cdot \bar{S}_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\bar{Z}_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

FUNCTION TABLE

Select Inputs		Inputs (a or b)					Output
S ₀	S ₁	\bar{E}	I ₀	I ₁	I ₂	I ₃	\bar{Z}
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

MC54/74F352

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCH}	Power Supply Current		9.3	14	mA	V _{IN} = GND	V _{CC} = MAX
I _{CCL}			13.3	20		V _{IN} = HIGH	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.5	7.4	11	3.0	14	3.0	12.5	ns
t _{PHL}	S _n to \bar{Z}_n	3.0	7.0	8.5	2.5	11	2.5	9.5	
t _{PLH}	Propagation Delay	2.5	5.0	7.0	2.0	10	2.0	8.0	ns
t _{PHL}	\bar{E}_n to \bar{Z}_n	3.0	5.0	7.0	2.5	9.0	2.5	8.0	
t _{PLH}	Propagation Delay	2.5	4.9	7.0	2.0	9.0	2.0	8.0	ns
t _{PHL}	I _n to \bar{Z}_n	1.5	3.0	3.5	1.0	5.0	1.0	4.0	